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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,451	03/07/2002	Chi Chang	SUND 295	9022

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EXAMINER	
BRINEY III, WALTER F	
ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 12/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,451	CHANG ET AL.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter that was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The current invention is directed solely to mitigating ringback caused by undershooting a line voltage during a transition from logic one to logic zero. As such, the constriction circuit of claim 5, whose details are depicted in figure 5, does not include any circuitry for lowering the resistance value of the constriction resistor when the output of the comparator transitions from low to high. For the purposes of this rejection, the examiner is interpreting the claim so that the constriction resistor's resistance is lowered during a transition from high to low.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. **Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art in view of Takeda (US Patent 6,326,803).**

Claim 1 is limited to *an apparatus of ring-back constriction, coupled to a transmission line, for constricting a ring-back effect.* Applicant's admitted prior art, shown in figure 2, includes a receiving *comparator* (203), which compares a received logic signal from *transmission line* (L) to a reference signal V_{ref}. The output is fed directly to *a termination controller* (202), which adjusts the resistance of *a variable terminating resistor* (R_t). The net effect is to provide temporary impedance matching. However, no reference to a constriction controller is made in this admitted prior art. Therefore, the applicant's admitted prior art of figure 2 anticipates all limitations of the claim with the exception of *a constriction controller.*

Takeda discloses a terminating circuit for a transmission line. See Abstract. In particular, the device reduces both the effects of overshoot and undershoot apparent in switching logic states between high and low levels. Figure 10 depicts a prior art termination circuit that is very similar to the applicant's own admitted prior art. In particular, inverter (116) corresponds to the *termination controller* and inverter (117) is the *termination resistor.* The prior art device of figure 10 suffers from large over and undershoots, and thus, benefits from the invention depicted by Takeda in figure 1. With respect to the current claim language, the first input inverter (16) corresponds to the first inverter (116) of figure 10 and the second inverter (17) corresponds to the second inverter (117). In addition to the termination provided by the PMOS (12) and NMOS

(13) transistors, the circuit of Takeda also includes *a constriction controller* comprising inverters (21, 22, and 23), PMOS transistor (32), and NMOS transistor (33). Constriction current is provided by way of PMOS (31) and NMOS (34), i.e. *a constriction variable resistor*, both of which are coupled to *a constriction voltage*. It would have been obvious to one of ordinary skill in the art to include the overshoot/undershoot mitigating circuitry (41) as taught by Takeda with the applicant's admitted prior art comprising a comparator and termination controller for the purpose of eliminating the overshoot/undershoot effects that arise due to impedance mismatches within a transmission line termination.

Claim 2 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. With regards to the logical response of the circuitry depicted in figure 1 of Takeda, a logical one on transmission line (4) will be inverted by inverter (16), thus producing a logical zero that controls PMOS (12) to enter the saturation state, i.e. *the termination variable resistor is of a low value*. It follows that when a logical zero is on the transmission line (4), the inverter (16) will output a logical one, thus causing PMOS (12) to cutoff, i.e. *the resistance of the termination variable resistor from low value to high value*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 3 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. All transistors have an inherent transition period from the saturation to the cut-off region, thus the PMOS transistor (12) of Takeda inherently *reaches a high value after a transition period*. Therefore, the

applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 4 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. With respect to the constriction circuit, or over/undershoot mitigating circuitry, (41) of figure 1, a logical one on transmission line (4) will cause PMOS transistor (31) to be in a cutoff state, i.e. *a high value*. Then, when a logical zero transition occurs, the transistor transitions to the saturation state, and at the same time, the value at node (27) is still held at logical zero, thus gate (32) is in saturation, i.e. *a low value*. Upon the logical zero propagating through delay circuit (20), gate (32) will switch to cutoff, i.e. *after a delay period, the resistance of the constriction variable resistor transits from low value to high value*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 5 is limited to *the apparatus according to claim 4*, as covered by the applicant's admitted prior art in view of Takeda. It follows from the interpretation laid out in the preceding section that after the delay period described in claim 4 that the resistance value reaches cutoff after an inherent *transition period*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 6 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. As seen in figure 1, the PMOS transistor (14) is responsible for generating a logical one control at node (25). All

PMOS devices inherently require a non-zero amount of time to fully charge their output node. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 7 is limited to *the apparatus according to claim 6*, as covered by the applicant's admitted prior art in view of Takeda. As just described in the rejection of claim 6, the transistor responsible for the cutoff of transistor (12) is PMOS transistor (14), i.e. *wherein the weak transistor is a PMOS transistor.* Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 8 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. Quite clearly, delay circuit (20) is specifically designed to take a long time in charging and discharging node (27). To that extent, the driving PMOS and NMOS transistors within each inverter (21, 22, and 23) are weak and require an inherent transition period to drive node (32) to an appropriate level to cutoff transistor (32). Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 9 is limited to *the apparatus according to claim 8*, as covered by the applicant's admitted prior art in view of Takeda. As just described in the rejection of claim 8, circuit (20) is designed to slowly charge node (27) to force the cutoff of device (32), thus requiring a *weak PMOS transistor.* Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 10 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. As seen in figure 1, the termination

inverter circuit (17) comprises *PMOS transistor* (12). Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 11 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. As seen in figure 1, the over/under voltage mitigating circuitry (30) comprises *PMOS transistors* (31 and 32). Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 12 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. The CMOS process disclosed by Takeda uses 3.3V, see figure 6 and 11, however, the CMOS process used by the applicant's admitted prior art is 1.5V, see paragraph 7. Since Takeda is added to the applicant's admitted prior art, it follows that the Takeda reference should be modified to use 1.5V CMOS logic. Thus, the reference voltage should also be the same as the prior art, which is *1 volt*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 13 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. The CMOS process disclosed by Takeda uses 3.3V, see figure 6 and 11, however, the CMOS process used by the applicant's admitted prior art is 1.5V, see paragraph 7. Since Takeda is added to the applicant's admitted prior art, it follows that the Takeda reference should be modified to use 1.5V CMOS logic, i.e. *a terminating voltage of 1.5 volts*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 14 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. When a logical zero signal is received the constriction voltage used is equal to V_{CC}, and when a logical zero is present the termination voltage used is equal to ground, typically zero, i.e. *wherein the constriction voltage is higher than the termination voltage*. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Claim 15 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. The prior art admitted by the applicant is designed under a 1.5V CMOS process, see paragraph 7, the circuitry disclosed by Takeda uses a 3.3V CMOS process, see figures 6 and 11, in general, certain tradeoffs are made between one voltage level and another, for example: power dissipation, speed, capacitive noise, etc... As such, the CMOS process is a matter of design choice, and it would have been obvious to one of ordinary skill in the art at the time of the invention to use a CMOS process of around 2.5 to 2.6V instead of the disclosed 1.5 and 3.3V processes of the applicant's admitted prior art and Takeda, respectively, since the applicant's disclosure has not specified that a process of 2.5 to 2.6V provides any advantage over previously known efforts.

Claim 16 is limited to *the apparatus according to claim 1*, as covered by the applicant's admitted prior art in view of Takeda. The applicant's admitted prior art is intended for use with *a GTL+ (Gunning Transistor Logic Plus) bus*, see paragraph 7. Therefore, the applicant's admitted prior art in view of Takeda makes obvious all limitations of the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
12/21/04

XU MEI
PRIMARY EXAMINER